James (Jim) H. Pomerene

Born June 22, 1920, Yonkers, N. Y; design engineer for the IAS computer with John von Neumann, and the IBM HARVEST system.

Education: BS, electrical engineering, Northwestern University, 1942.

Professional Experience: design engineer, Hazeltine Corp., 1942-1946; Electronic Computer Project, Institute for Advanced Study: staff member, 1946-1951, chief engineer, 1951-1956; IBM Corp.: senior engineer, 1956-1976, IBM Fellow, 1976-present.

Honors and Awards: fellow, IEEE, 1971; Computer Pioneer Award, IEEE Computer Society, 1986; member, National Academy of Engineering, 1988; IEEE Edison Medal, 1993.

James H. Pomerene was born in Yonkers, New York, on June 22, 1920. After receiving his BS degree in electrical engineering from Northwestern University in June 1942, he joined the Hazeltine Corporation and was involved with the design of IFF radar, working in both the microwave and pulse modulator areas.

In April 1946 he accepted an invitation from John von Neumann and Herman Goldstine to join the newly organized Electronic Computer Project at the Institute for Advanced Study in Princeton, New Jersey. This project was to build a parallel stored-program computer that would be the prototype for a number of machines such as the MANIAC, ORACLE, ILLIAC, AVIDAC, and so on. Pomerene designed the adder portion of the arithmetic unit and then was entirely responsible for the development and construction of the electrostatic (Williams tube) memory. In August 1951 he was appointed chief engineer of the project, a position he held until the project was disbanded in 1956.

In July 1956 he joined the IBM Corporation in Poughkeepsie, New York, to work on the STRETCH project. He and several others conducted a study that began the development of the HARVEST computer, and he was subsequently put in charge of the design team. HARVEST was a special system built for the National Security Agency. It consisted of a STRETCH computer to provide standard computer processing, plus a byte vector pipeline unit for processing large amounts of nonnumeric data. HARVEST was unusual in several ways. It had two levels of program control: one level set up a process, including the pattern for fetching and storing bytes from and to memory; and the second level operated on the process set up by the first. It also had a remarkable tape and tape library system that was fully automatic and of great capacity.

Following the completion of HARVEST in 1962, Pomerene spent a year in IBM Research studying the use of multiple processors as a way to increase both computer capacity and system availability. He returned to Poughkeepsie to help with several contract proposals to the government, including a possible second HARVEST and a multiprocessor system, starting a chain of events that led to IBM's first commercial MP system, the Mod 65MP In 1965 he headed a team doing the preliminary design of the Parallel Network Digital Computer (PNDC), an early SIMD machine proposal. The PNDC was not built, but work on it led Pomerene to the idea of making a highly available memory system out of a number of memory units, each storing but one bit position of a word.

With top management support Pomerene began, in 1966, a special study of a highly available system based on this memory. As envisioned, the memory would read out a block of words on every access and it was

conjectured that such a block readout could be useful if each processor in the system were provided with a local memory capable of holding a number of recently used blocks. This arrangement, now known as a cache, was simulated and the results were much better than expected. Subsequently the cache was incorporated in the Model 85 processor.

In 1967 Pomerene was promoted to the position of senior staff member on the Corporate Technical Committee at corporate head quarters in Armonk, New York. He was appointed an IBM fellow in 1976 and soon transferred to the Research Division. He helped to found the High End Machine project in Research and is currently heading a group investigating a number of improvements in high-end 370 processor organization. Results of this work have contributed to high-end processor developments and have led to several important patents.

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UPDATES

James Pomerene died December 7, 2008 (MRW, 2012)